For the SPE Reference

IN THE CLAIMS

1-9. (Canceled)

10. (Currently Amended) A transistor formed in a semiconductor substrate, the substrate having a first conductivity type and a surface, the transistor comprising:

a collector region having an impurity therein which promotes one of either holes or electrons as a majority carrier, the collector region extending downward from the surface of the substrate, wherein the first conductivity type of the substrate promotes the other of either holes or electrons as a majority carrier;

a base region having an impurity therein which promotes the other type of carrier, the base region having a surface area and extending downward from the surface of the substrate into contact with a portion of the collector region;

an emitter on top of the base region and having a surface area, which is in contact with the base region, smaller than the surface area of the base region; and

an implant area of the collector region vertically adjacent to the base region having an increased collector doping of an implanted impurity, the implant area having an effective surface area, which is in contact with the base region, greater than the surface area of the emitter and less than the surface area of the base region.

11. (Previously Presented) The transistor of claim 10, wherein the transistor is an NPN transistor and the implant impurity in the implant area of the collector region is phosphorous.

12. (Previously Presented) The transistor of claim 10, wherein the transistor is a PNP transistor and the implant impurity in the implant area of the collector is boron.

13. (Currently Amended) A transistor formed in a semiconductor substrate, the substrate including a surface and a region doped with an impurity which promotes one of either holes or electrons as a first majority carrier, the transistor comprising:

a collector region having an impurity therein which promotes the other of holes or electrons as a second majority carrier, the collector region extending from the surface of the substrate;

a base region having an impurity therein which promotes the first majority carrier, the base region extending from the surface of the substrate into contact with a portion of the collector region;

an emitter region on the base region, the emitter region having a surface area that is in contact with the base region and is smaller than a surface area of the base region; and

an implant region interposed between the collector region and the base region, the implant region having an increased doping of an implant impurity and having an effective surface area greater than the surface area of the emitter region and less than the area of the base region contiguous to the collector region, wherein the effective surface area is in contact with the base region.

14. (Previously Presented) The transistor of claim 13, wherein the transistor is an NPN transistor and the implant impurity in the implant region is phosphorous.

15. (Previously Presented) The transistor of claim 13, wherein the transistor is a PNP transistor and the implant impurity in the implant region is boron.

16. (Previously Presented) The transistor of claim 13, wherein the effective surface area of the implant region minimizes carrier injection from the emitter region to the collector region outside of the implant region at high current operation of the transistor.

17. (Currently Amended) A transistor formed in a semiconductor substrate, the substrate including a surface and a region doped with an impurity which promotes one of either holes or electrons as a first majority carrier, the transistor comprising:

a collector region having an impurity therein which promotes the other of holes or electrons as a second majority carrier, the collector region extending from the surface of the substrate;

a base region having an impurity therein which promotes the first majority carrier, the base region extending from the surface of the substrate into contact with a portion of the collector region;

an emitter region on the base region, the emitter region having a surface area smaller than a surface area of the base region;

a first implant region interposed between the collector region and the base region, the implant region having an increased doping of an implant impurity and having an effective surface area greater than the surface area of the emitter region contiguous to the base region and less than the area of the base region contiguous to the collector region; and

a second implant region formed in the collector region.

18. (Previously Presented) The transistor of claim 17, wherein the second implant region is formed at about the same level from the surface of the substrate as the first implant.

19. (Previously Presented) The transistor of claim 17, wherein the collector region includes a plug extending from the surface of the substrate, the plug being separate from the base region.

20. (Previously Presented) The transistor of claim 19, wherein the second implant region is formed in the plug at about the same level from the surface of the substrate as the first implant region.

21. (Previously Presented) The transistor of claim 17, wherein the transistor is an NPN transistor and the implant impurity in the first and second implant regions is phosphorous.

22. (Previously Presented) The transistor of claim 17, wherein the transistor is a PNP transistor and the implant impurity in the first and second implant regions is boron.

23. (Previously Presented) The transistor of claim 17, wherein the effective surface area of the first implant region minimizes carrier injection from the emitter region to the collector region outside the first implant region at high current operation of the transistor.

24. (Previously Presented) The transistor of claim 17, wherein the second implant region has a surface area greater then the area of an opening through which the second implant region is formed.

25. (Currently Amended) A transistor, comprising:

an emitter having an emitter surface area;

a base having a base surface area, wherein the emitter surface area is in contact with the base;

a collector in contact with the base; and

an implant region intermediate the base and the collector, the implant region having an implant surface area in contact with the base, the implant surface area being greater than the emitter surface area and less than the base surface area.

26. (Previously Presented) The transistor of claim 25 wherein the collector has a collector surface area, and the implant region surface area is less than the collector surface area.

27. (Previously Presented) The transistor of claim 26, wherein the base surface area is less than the collector surface area.

28. (Previously Presented) The transistor of claim 26, wherein the base surface area and the implant region surface area where both contact the collector have a combined area greater than the emitter surface area.

29. (Previously Presented) The transistor of claim 26, wherein the base directly contacts both the collector and the implant region.

30. (Previously Presented) A transistor device formed in a semiconductor substrate comprising:

a diffused n well collector region having an impurity of a first conductivity type, the collector region extending downwardly from a surface of the substrate, the substrate being generally doped with an impurity of a second conductivity type;

a base region having an impurity of the second conductivity type doped at a generally constant doping level across a surface thereof, the base region extending downwardly from the surface of the substrate into contact with a portion of the collector region;

an emitter having an impurity of the first conductivity type on top of the base region and having a surface area smaller than a surface area of the base region; and

an area of the collector region vertically adjacent the base region having an increased collector doping of the first conductivity type, the area of the collector region having an effective surface area in contact with the base region that is greater than the surface area of the emitter.

31. (Previously Presented) The transistor device of claim 30, wherein the impurity of the first conductivity device is phosphorous.

32. (Previously Presented) The transistor device according to claim 30, wherein the effective surface area of the collector region is less than a non-increased doped area of the portion of the collector region in contact with the base region.

33. (Currently Amended) A transistor formed in a substrate, the substrate having a first conductivity type and a surface, the transistor comprising:

a collector region having a first impurity means for promoting one of either holes or electrons as a majority carrier, the collector region extending downward from the surface of the substrate, wherein the first conductivity type of the substrate promotes the other of either holes or electrons as a majority carrier;

a base region having a second impurity means for promoting the other type of carrier, the base region having a surface area and extending downward from the surface of the substrate into contact with a portion of the collector region;

an emitter region on top of the base region and having a surface area smaller than the surface area of the base region; and

an implant area of the collector region vertically adjacent to the base region having an increased collector doping of an implanted impurity, the implant area having an effective surface area that is in contact with the base region, greater than the surface area of the emitter region and less than the surface area of the base region.

34. (Currently Amended) A transistor, comprising:

an emitter having an emitter surface area;

a base having a base surface area, wherein the emitter surface area is in contact with the base;

a collector in contact with the base;

a collector plug in the collector;

a first implant region intermediate the base and the collector, the first implant region having an implant surface area in contact with the base, the implant surface area being greater than the emitter surface area and less than the base surface area; and

a second implant region in the collector plug.

35. (Previously Presented) The transistor of claim 34, wherein the first implant region and the second implant region are positioned at a same depth.

36. (Previously Presented) The transistor of claim 34, wherein the first implant region and the second implant region are simultaneously formed by an angled implant such that areas of the first implant region and the second implant region are greater than areas of the openings through which the first implant region and the second implant region are formed.

37. (Previously Presented) The transistor of claim 34, wherein the first implant region and the second implant region are doped by a same source.

38. (Currently Amended) A transistor, comprising:

an emitter having a periphery;

a base in contact with the emitter to define an emitter-base surface;

a collector in contact with the base; and

means for minimizing carrier injection from the periphery of the emitter region to the collector region at high current operation of the transistor, wherein the means includes a region in contact with the collector and the base, the region including a first surface in contact with the base and a second surface in contact with the collector, the first surface being larger than the emitter-base surface.

39. (Canceled)

40. (Currently Amended) A transistor, comprising:

an emitter;

a base in contact with the emitter to define an emitter-base surface;

a collector in contact with the base; and

means for minimizing base-collector capacitance and maximizing high current operation, wherein the means includes a region in contact with the collector and the base, the region including a first surface in contact with the base and a second surface in contact with the collector, the first surface being larger than the emitter-base surface.

41. (Canceled)